IN THE CLAIMS

We claim:

1. A transistor comprising:

a gate electrode formed on a gate dielectric layer formed on a substrate;

a pair of source/drain regions formed in said substrate on opposite sides of said laterally opposite sidewalls of said gate electrode; and

wherein said gate electrode has a central portion formed on the gate dielectric layer over the substrate region between said source/drain regions and a pair of sidewall portions which overlap a portion of said source/drain regions wherein said central portion has a first work function and said pair of sidewall portions has a second work function, wherein said second work function is different than said first work function.

2. The transistor of claim 1 wherein said source/drain regions are n type conductivity and wherein said central portion has a second work function of between 3.9 to 4.3 eV.

3. The transistor of claim 2 wherein said sidewall portions of said gate electrode has a work function of between 1.5 to 3.8 eV.

4. The transistor of claim 1 wherein said source/drain regions are formed of n type conductivity and said outside portion has a first work function which is at least 0.1 eV lower than said central portion.

5. The transistor of claim 1 wherein said source/drain region are formed of p type conductivity and wherein said central portion has a work function of between 4.9 to 5.3 eV.

6. The transistor of claim 5 wherein said sidewall portions has a work function of between 5.4 to 6.0 eV.

7. The transistor of claim 1 wherein the source/drain regions are p type conductivity and said sidewall portions have a work function that is at least 0.1 eV higher than the work function of said central portion.

8. The transistor of claim 1 wherein the source/drain regions are n type conductivity and wherein said sidewall portions of said gate electrode are formed from a material selected from the group consisting of scandium (Sc), magnesium (Mg) and Yttrium (Y).

9. The transistor of claim 1 wherein the source/drain regions are n type conductivity and the central portion of said gate electrode comprises a conductive material selected from the group consisting of poly-silicon, titanium, zirconium, hafnium, tantalum, and aluminum.

10. The transistor of claim 1 wherein said source/drain regions are p type conductivity and wherein said sidewall portions of said gate electrode comprises a conductive material that is selected from the group consisting of poly-silicon, platinum, and ruthenium nitride (RuN).

11. The transistor of claim 1 wherein said source/drain region are p type conductivity and said central portion is formed from a material selected from the group consisting of ruthenium and palladium.

12. A method of forming a transistor comprising:

forming an opening in a dielectric film over a semiconductor substrate, said opening having a first and second laterally opposite sidewalls formed over a pair of source/drain

regions formed in said substrate, said opening having a central portion formed over said substrate between said source/drain regions;

forming a gate dielectric layer over said substrate in said opening;

depositing a first conductive material having a first work function at a first angle adjacent onto said gate dielectric and to said first sidewall of said opening;

sputter depositing said first conductive material at a second angle onto said gate dielectric layer and adjacent to said second laterally opposite sidewalls; and

depositing a second conductive material having a second work function into said central portion of said opening on said gate dielectric layer over said channel region.

13. The method of claim 12 wherein said first angle is different than said second angle.

14. The method of claim 13 wherein said second angle is greater than said first angle.

15. The method of claim 12 wherein after depositing said first conductive film on said first and second sidewalls, exposing said first conductive material to a reactive species to alter said first work function.

16. The method of claim 15 wherein said reactive species are generated or provided by a process selected from the group consisting of plasma generation, ion implantation, and thermal activation.

17. The method of claim 15 wherein said reactive species increase the work function of said first conductive material.

18. The method of claim 15 wherein said reactive species decrease the work function of said first conductive material.

19. A method of forming a transistor comprising:

forming an opening in a dielectric film over a semiconductor substrate, said opening having first and second laterally opposite sidewalls formed over a pair of source/drain regions formed in said substrate and a central portion formed over a channel region between said source/drain regions;

forming a gate dielectric layer over said semiconductor substrate in said opening;

depositing a first conductive material having a first work function over said top surface of said dielectric film, adjacent to said first and second sidewalls and on said gate dielectric layer in said opening;

anisotropically etching said first conductive material so as to remove said first conductive material from the top surface of said interlayer dielectric and from the central portion of said opening to form a pair of sidewall portions adjacent to said first and second sidewalls; and

depositing a second conductive material having a second work function onto said gate dielectric layer in said central portion of said opening over said gate dielectric layer wherein said second work function is different than said first work function.

20. The method of claim 19 wherein said first metal film is conformally deposited.

21. The method of claim 20 wherein said first metal film is deposited by a method selected from the group consisting of chemical vapor deposition and atomic layer deposition.

22. The method of claim 19 wherein said first conductive material is exposed to reactive species to change the work function of said first conductive material.

23. The method of claim 19 wherein said first work function is lower than said second work function.

24. The method of claim 19 wherein said first work function is greater than said second work function.

25. A transistor comprising a gate electrode formed on a gate dielectric layer formed on a substrate.

26. A method of forming a transistor comprising:

forming a gate electrode on a gate dielectric layer on a substrate wherein said gate electrode has a pair laterally opposite sidewalls and a central portion wherein the laterally opposite sidewalls have a first work function and the central portion has a second work function wherein the first work function is different than the second work function; and

a pair of source/drain regions formed in said substrate on opposite sides of said laterally opposite sidewalls of said gate electrode wherein a portion of said source/drains regions are formed beneath said laterally opposite sidewalls.

27. The method of claim 26 wherein said source/drain regions are formed of n type conductivity and wherein said first work function is less than said second work function.

28. The method of claim 26 wherein said source/drain regions are p type conductivity and wherein said first work function is greater than said second work function.